IN THE CLAIMS:

1. (Currently Amended) A self orthogonal code decoding circuit for ~~performing~~ decoding ~~for~~ a self orthogonal code and repeating decoding ~~for~~ of said self orthogonal code for a plurality of times, using a plurality of decoding stages, wherein for each of said plurality of stages, a reception series error detection threshold value for detecting a reception series error is set to a predetermined value and in a first decoding stage, said reception series error detection threshold value is set high for detecting a reception series error only if there is a high probability of error and the threshold values are gradually lowered in each successive decoding stage, for error detection when there is a lower probably of error.

2. (Currently Amended) A self orthogonal code decoding circuit for ~~performing~~ decoding for a self orthogonal code on the basis of a syndrome bit determined ~~only~~ by an error in a reception series which ~~is~~ was generated ~~by adding error to~~ from a transmission series, which ~~is~~ was in turn generated by a parallel/serial conversion ~~with~~ and by adding a check series to an information series, comprising:

a plurality of decoding circuit stages ~~of deciding circuit~~ for repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times; and

a check series register output provided ~~for~~ from each decoding circuit stage except ~~for the~~ from a final decoding circuit stage, ~~at a final stage among said plurality of stages of decoding circuits and~~ for inputting said check series to the next ~~stage of~~ decoding circuit stage with a delay.

3. (cancelled)

4. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim ~~2~~ 1, which comprises means for performing a code synchronization ~~judgment~~ error detection by counting the number of detected reception series errors ~~as being judged as error~~ and performing code synchronization error detection on the basis of the counted ~~error~~ number of detected errors.

5. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim ~~3~~ 1, which comprises a code synchronization dedicated ~~threshold value judgment~~ error detection circuit provided separately from ~~the~~ a circuit for ~~making judgment of~~ said reception series error detection ~~and dedicated for code synchronization and making judgment whether~~ for detecting a synchronization error ~~is caused or not~~ on the basis of ~~threshold value judgment~~ a threshold value optimized for code synchronization error detection, ~~and said threshold value of~~ said code synchronization dedicated error detection threshold value ~~judgment circuit to be~~ being lower than said ~~threshold value~~ reception series error ~~judgment~~ detection threshold value.

6. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 5, which comprises a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ error detection circuit, so as not to perform reception series error correction on the basis of the result of error ~~judgment of~~ detection by said code synchronization dedicated ~~threshold value judgment~~ error detection circuit ~~for said syndrome register~~.

7. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 4, wherein each decoding circuit in said plurality of stages comprises:

a syndrome generation means for generating said syndrome bit;

an error value generation means for ~~leading~~ generating an error value by ~~making judgment of~~ detecting an error of said syndrome bit generated by said syndrome generation means, on the basis of said reception series error detection threshold value ~~judgment threshold value~~

an error correcting means for correcting an error of said syndrome bit on the basis of said error value generated by said error value generation means; and

an error detection counter for counting errors on the basis of said error value generated by said error value generation means.

8. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 1, ~~wherein~~, in a system including

an information source generating an information series,

an encoder for converting said information series into a code series, and

a communication path for transmitting said code series~~, decoding for said self orthogonal code is repeated for a plurality of times~~.

9. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 8, wherein said communication path is constructed with a wired cable.

10. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 9, wherein said wired cable is an optical cable.

11. (Currently Amended) A self orthogonal code decoding circuit as set forth in claim 8, wherein said communication path is a transmission path in radio communication.

12. (Currently Amended) A self orthogonal code decoding method for ~~performing~~ decoding ~~for~~ of a self orthogonal code and repeating decoding ~~for~~ of said self orthogonal code ~~for~~ a plurality of times, using a plurality of decoding stages, wherein for each of said plurality of stages, a reception series error detection threshold value for detecting a reception series error is set to a predetermined value and in a first decoding stage, said reception series error detection threshold value is set high for detecting a reception series error only if there is a high probability of error and the threshold values are gradually lowered in each successive decoding stage, for error detection when there is a lower probably of error.

13. (Currently Amended) A self orthogonal code decoding method for ~~performing~~ decoding ~~for~~ a self orthogonal code on the basis of a syndrome bit determined ~~only~~ by an error in a reception series which ~~is~~ was generated ~~by adding error to~~ from a transmission series which ~~is~~ was in turn generated by a parallel/serial conversion ~~with~~ and by adding ~~an~~ a check series to an information series, comprising a step of:

in each of a plurality of decoding circuit stages ~~of deciding circuit~~ for repeating decoding ~~for~~ of said self orthogonal code for a plurality of times, said check series ~~being~~ is input to a next decoding circuit stage ~~of decoding circuit~~ with a delay, except ~~for~~

from the ~~decoding circuit at the~~ final decoding circuit stage.

14. (cancelled)

15. (Currently Amended) A self orthogonal code decoding method as set forth in claim ~~13~~ 12, which comprises means for performing code synchronization ~~judgment~~ error detection by counting the number of detected reception series errors ~~as being judged as error~~ and performing code synchronization error detection on the basis of the counted ~~error~~ number of errors.

16. (Currently Amended) A self orthogonal code decoding method as set forth in claim 15, wherein a threshold value of a code synchronization dedicated ~~threshold value judgment~~ error detection circuit is provided separately from the circuit for ~~making judgment of said error~~ reception series error detection and dedicated ~~for~~ to code synchronization error detection ~~and making judgment whether error is caused or not~~ on the basis of ~~threshold value judgment~~ a threshold value optimized for code synchronization~~,~~ error detection being set lower than said reception series error detection threshold value ~~judgment threshold value~~.

17. (Currently Amended) A self orthogonal code decoding method as set forth in claim 16, which comprises a step of providing a syndrome register which shifts said syndrome bit ~~provided for code synchronization to output~~ to said code synchronization dedicated ~~threshold value judgment~~ error detection circuit, so ~~as~~ not to perform reception series error correction on the basis of the result of error detection by ~~judgment of~~ said code

synchronization dedicated ~~threshold value judgment~~ error detection circuit ~~for said syndrome register.~~

18. (Currently Amended) A self orthogonal code decoding method as set forth in claim 15, which includes

~~step of~~ generating said syndrome bit,

~~step of leading~~ generating an error value by ~~making judgment of~~ detecting an error of said syndrome bit generated by said syndrome generation means on the basis of said ~~threshold value judgment~~ reception series error detection threshold value,

~~step of~~ correcting the error of said syndrome bit on the basis of said error value generated by said error value generation means;

and ~~step of~~ counting said error number on the basis of said error value generated by said error value generation means.

19. (Currently Amended) A self orthogonal code decoding method as set forth in claim 12, ~~wherein,~~ in a system including

an information source for generating an information series,

an encoder for converting said information series into a code series, and

a communication path for transmitting said code series~~, decoding for said self orthogonal code is repeated for a plurality of times~~.

20. (Currently Amended) A self orthogonal code decoding method as set forth in claim 19, wherein said communication path is constructed with a wired cable.

21. (Currently Amended) A self orthogonal code decoding method as set forth in claim 20, wherein said wired cable is an optical cable.

22. (Currently Amended) A self orthogonal code decoding method as set forth in claim 19, wherein said communication ~~oath~~ path is a transmission path in radio communication.